AMENDMENTS IN THE SPECIFICATION

Please amend the paragraph starting on page 15, line 16 as follows:

Once an initial value for the primary scrambling code is applied to the first and second shift register memories 700 and 705 each having 18 registers for cyclically shifting the register value "a_i" or "b_i", the 0-th register values of the first and second shift register memories 700 and 705 are fed into the adder 740 and the 18 register values "a_i" of the first shift register memory 700 are fed into the first to N-th masking sections 710 to 712 in order to generate cyclically shifted sequences of the first shift registers. Meanwhile, the 18 register values "b_i" of the second shift register memory 705 are fed into the first to N-th masking sections 714 to 716 in order to generate cyclically shifted sequences of the first shift registers. Then, the first masking section 710 masks the input values from the first (upper) shift register memory 700 (all 18 bits from 18 registers in the shift register memory 700) with a mask function k^1_i (i.e., $\sum(k^1_i \times a_i)$) and outputs the masked values to the summer 744 for generating the first secondary scrambling code. The masking is concurrently processing in every masking sections 710 – 712. The N-th masking section 712 masks the input values from the first (upper) shift registers with a mask function k^N_i (i.e., $\sum(k^N_i \times a_i)$) and outputs the masked values to the summer 742 for generating the N-th secondary scrambling code. The N-th masking section 716 masks the input values from the second (lower) shift registers with a mask function s^N_i (i.e., $\sum(s^N_i \times a_i)$) and outputs the masked values to the summer 744 for generating the N-th secondary scrambling code. The first masking section 714 masks the input values from the register memory 705 with a mask function s^1_i (i.e., $\sum(s^1_i \times a_i)$) and outputs the resulting values to the adder 742 for generating the first secondary scrambling code. Each of the masking sections 710 – 712 masks the input values from the first shift register memory 700 and outputs the masked value to the respective adders 742 – 744. Then, the adder 740 adds the output bits from the 0-th registers of the first and second shift register memories 700 and 705. These generated output signals are immediately delayed at the delay 720. The adder 744 adds the output bits from the N-th masking sections 712 and 716 to generate I-channel signals, which are immediately fed into the delay 724. The delay 722 delays the I-channel signals output from the adder 742 ~~744~~ for a predetermined number of chips to generate Q-channel scrambling

signals. The adder 742 adds the output bits from the first masking sections 710 and 714 to generate I-channel signals. These I-channel signals are immediately delayed for a predetermined number of chips at the delay 722. Then, the 0-th and seventh register values of the first shift register memory 700 are added at the summer 730 and the added value is inputted to the seventeenth register, as the left-sided values are shifted to the right side by one and the utmost left-sided register is newly filled with the output value of the summer 730. The 0-th, fifth, seventh, and tenth register values of the second shift register memory 705 are added at the adder 735, the added value is inputted into the seventeenth register, as the left-sided values are shifted to the right side by one and the utmost left-sided register (i.e., the seventeenth register) with the output value of the summer 735. This procedure is repeated to generate multiple scrambling codes.